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[54] **PHYSICAL ADDRESS SIZE SELECTION AND PAGE SIZE SELECTION IN AN ADDRESS TRANSLATOR**

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[56] **References Cited**

U.S. PATENT DOCUMENTS

4,340,932	7/1982	Bakula et al.	395/402
4,432,053	2/1984	Gaither et al.	395/416
4,654,777	3/1987	Nakamura	395/416
4,669,043	5/1987	Kaplinsky	395/403
4,679,140	7/1987	Gotou et al.	395/775
4,758,946	7/1988	Shar et al.	395/416
4,763,250	8/1988	Keshlear et al.	395/418
4,792,897	12/1988	Gotou et al.	395/417
4,835,734	5/1989	Kodaira et al.	395/419
4,972,338	11/1990	Crawford et al.	395/416
4,979,098	12/1990	Baum et al.	395/418
5,023,777	6/1991	Sawamoto	395/402
5,263,140	11/1993	Riordan	395/417
5,475,827	12/1995	Lee et al.	395/417

FOREIGN PATENT DOCUMENTS

0113240	12/1983	European Pat. Off. .
1595740	5/1978	United Kingdom .
2127994	6/1983	United Kingdom .

OTHER PUBLICATIONS

Data General MV 2000, Chapter 3, *Logical To Physical Address Translation;* pp. 32–37 (publication information unknown).

i860™ Microprocessor Family Programmer's Reference Manual, Intel Corporation Literature Sales, P.O. Box 7641, Mt. Prospect, Ill 650056–7641, Chapter 4, pp. 1–13, 1991.

Patterson, David A. and John L. Hennessey, *Computer Architecture A Quantative Approach,* Morgan Kaufman Publishers, Inc., San Mateo, California pp. 432–485.

(List continued on next page.)

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[57] **ABSTRACT**

An address translator and a method for translating a linear address into a physical address for memory management in a computer is described herein. Different memory sizes, and different page sizes can be selected. The address translator can translate from a standard 32-bit linear address for compatibility with previous 32-bit architectures, and can also translate to a physical memory size with a larger physical address than linear address; i.e., greater than 32 bits (e.g. 36 bits and up), with no increase in access time. The address translator translates a linear address that includes an offset and a plurality of fields used to select entries in a plurality of tables. The format of the linear address into fields is dependent upon the selected memory size and the selected page size. For a large memory size, the tables include a directory pointer table that includes a group of directory pointers, a plurality of page table directories each of which includes a group of page directory entries, and a plurality of page tables each of which includes a group of page table entries. The size of the entries in the tables is dependent upon the selected memory size. The contents of the tables are stored in memory, and furthermore the pointer table is stored in both main memory and in dedicated pointer table registers.

28 Claims, 12 Drawing Sheets